A Novel Drain Current *I–V* Model for MESFET

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***Abstract*—The conventional approach for modeling the dc *I–V* characteristics of a MESFET transistor usually adopts the hyperbolic tangent dependence on $V_{\rm ds}$. On the contrary, our new empirical model describes the device drain current as a polynomial of effective gate–source voltage $V_{\rm eff}$. The derived model is capable of accurately model the subthreshold effect and the device current–voltage behavior at different operating regions, in particular, the device operation around the pinchoff region. Measured and modeled results of a 0.5-μm gatelength MESFET device are compared and good agreement has been obtained. Comparisons between the proposed model, Curtice model, Chalmers model, and Parker model are also made in this paper. In addition, a single-stage class-AB amplifier was built with a commercial high-power MESFET transistor to verify the new model.**

***Index Terms*—Large-signal model, MESFET, nonlinear model.**

I. Introduction

AN ESSENTIAL prerequisite for computer-aided design (CAD) software to obtain a reliable design is the existence of an accurate nonlinear model for active device. A variety of analytical models [1]–[4] have been developed to describe the operation characteristics of a MESFET. All of these models are capable of expressing the device properties with only some success in a certain region of device operation.

Among these nonlinear characteristics, the most important one is the drain–source current performance with respect to drain–source and gate–source voltages. Conventional models [1]–[4] usually assume the drain current equation as the product of the following two functions:

$$I_{\rm ds}\left(V_{\rm gs},V_{\rm ds}\right)=F_1\left(V_{\rm gs},V_{\rm ds}\right)\cdot F_2\left(V_{\rm gs},V_{\rm ds}\right) \tag{1}$$

where both F_1 and F_2 are functions of $V_{\rm gs}$ and $V_{\rm ds}$. The first function is mainly aimed at describing the drain current variation with gate voltage. The second term, which adopts a hyperbolic function, focuses on the modeling of drain current variation with drain voltage.

In this paper, instead of using (1), a new drain current model is proposed. The drain current is now modeled as a third-order polynomial of effective gate–source voltage $V_{\rm eff}$, which, in turn, is described by a rational function of $V_{\rm gs}$. The model equation is unique and simple. In addition, it is very accurate in various device operation regions. In particular, the performance prediction close to pinchoff region is greatly improved.

A submicrometer wafer MESFET device and a Fujitsu FLC103WG packaged high-power MESFET transistor are adopted to verify the proposed model. A simple single-stage class-AB amplifier was built with a Fujitsu FLC103WG high-power device to verify the new model. The simulation and measurement results of the intermodulation distortion of this amplifier are compared.

II. New Large-Signal Model

In this paper, the drain current characteristic assumes the following form:

$$\begin{aligned}I_{\rm ds}=b_1V_{\rm ds}V_{\rm eff}^3&+\frac{b_4V_{\rm ds}\left(b_2+b_3V_{\rm ds}\right)V_{\rm eff}^2}{\sqrt{\left(1+gV_{\rm gst}\right)^2+V_{\rm ds}^2\left(b_2+b_3V_{\rm ds}\right)^2}}\\&+\frac{b_5V_{\rm ds}\left(b_2+b_3V_{\rm ds}\right)V_{\rm eff}}{\sqrt{\left(1+gV_{\rm gst}\right)^2+V_{\rm ds}^2\left(b_2+b_3V_{\rm ds}\right)^2}}\end{aligned} \tag{2}$$

where

$$\begin{aligned}V_{\rm gst}&=V_{\rm gs}-V_{TO}+\gamma V_{\rm ds}\\V_{\rm eff3}&=0.5\Big(V_{\rm gst}\left(1+c_{\rm pin}\right)+\sqrt{V_{\rm gst}^2+V_{ST}^2}\left(1-c_{\rm pin}\right)\Big)\\V_{\rm eff}&=V_{ST}\left(1+M_{VST}V_{\rm ds}\right)\ln\left(1+e^{V_{\rm eff3}/\left(V_{ST}\left(1+M_{VST}V_{\rm ds}\right)\right)}\right).\end{aligned} \tag{3}$$

V_{TO} is the pinchoff voltage, γ, b_1, b_2, b_3, b_4, b_5, g, V_{ST}, M_{VST}, and $c_{\rm pin}$ are the model parameters that are introduced to improve the subthreshold and pinchoff regions and, finally, $V_{\rm gs}$ and $V_{\rm ds}$ are the intrinsic terminal voltages.

Applying a large negative gate potential to an FET never succeeds in completely cutting off the drain current, as the channel mobile carrier density declines less rapidly than that predicted from the abrupt depletion approximation. Near pinchoff, the current diminishes exponentially with gate potential and will increase when gate-drain breakdown occurs [6]–[8]. The transformation of $V_{\rm gs}$ into effective gate–source voltage $V_{\rm eff}$ through (2) accurately describes the device operation around the pinchoff region. This transformation is well behaved and infinitely differentiable. Thus, it serves to be a good representation for intermodulation characteristics.

III. Model Parameter Extraction

A 2 × 150 μm submicrometer gatelength MESFET device (wafer device) and a Fujitsu FLC103WG packaged high-power MESFET transistor are used to verify the new model. The S-parameter data are measured at a multibias condition. The small-signal equivalent-circuit models are extracted under a multibias condition using the cold FET method combined with a multiplane data-fitting approach [9]. All the parasitic element values are kept constant in the large-signal model. The extracted parasitic element values are listed in Tables I and II, respectively,

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TABLE I
PARASITIC ELEMENT VALUES FOR WAFER DEVICE

C_{pg}(fF)	C_{pd}(fF)	L_g(pH)	L_d(pH)
32.9	30.1	155.4	160.6
L_s(pH)	R_s(Ω)	R_g(Ω)	R_d(Ω)
3.0	2.1	5.9	4.3

TABLE II
PARASITIC ELEMENT VALUES FOR FUJITSU FLC103WG

C_{pg}(pF)	C_{pd}(pF)	L_g(nH)	L_d(nH)
1.31	0.436	1.49	1.29
L_s(pH)	R_s(Ω)	R_g(Ω)	R_d(Ω)
59.5	0.99	1.53	1.96

TABLE III
MODEL PARAMETERS FOR WAFER DEVICE

V_{TO} (V)	γ	V_{ST}	b_1	b_2	b_3
-1.21	0.0358	0.103	-0.71	2.783	4.235
b_4	b_5	g	M_{VST}	cpin	
14.31	23.96	0.196	0.162	1.562	

TABLE IV
MODEL PARAMETERS FOR THE FUJITSU FLC103WG

V_{TO} (V)	γ	V_{ST}	b_1	b_2	b_3
-2.28	9.16e-3	0.436	-4.85	0.78	0.241
b_4	b_5	g	M_{VST}	cpin	
102.4	221.86	-0.136	-0.068	4.87	

for the two devices. The large-signal model parameters are extracted from the drain current *I–V* data at the intrinsic device plane and are listed in Tables III and IV, respectively, for the two devices. All the parameter extractions are performed by in-house developed software running under MATLAB. A simplex algorithm is used for the optimization.

IV. MODELING RESULTS AND DISCUSSIONS

The model parameters for the 2 × 150 μm submicrometer gatelength on-wafer MESFET device are extracted for the Curtice model [1], Chalmers model [2], Parker model [5], and the new model. These results are clearly plotted in Fig. 1 together with the measured data.

As observed from Fig. 1, the fitting error for Curtice model [1] is quite significant in the linear, knee, and saturation regions, especially as the drain current is reduced. It also has a conditional cutoff in the pinchoff region. The Chalmers model [2] offers an improvement over the Curtice model, but the fitting of the Chalmers model in the knee and saturation regions and for small drain current is still poor. Both the Parker model [5] and proposed new model give very accurate fitting results over various device operation regions. The small negative $I_{\rm ds}$–$V_{\rm ds}$ slope for large $I_{\rm ds}$ is well described by our model. The modeled drain current goes smoothly to zero when $V_{\rm gs}$ approaches or drops below pinchoff. Our model also gives an accurate subthreshold modeling, as depicted in Fig. 2.

Fig. 3 gives the comparison between the measured and simulated $I_{\rm ds}$–$V_{\rm gs}$ and g_m–$V_{\rm gs}$ characteristics of the same wafer device. The measured and simulated g_m results near the pinchoff region of the same device are presented in Fig. 4. Figs. 5

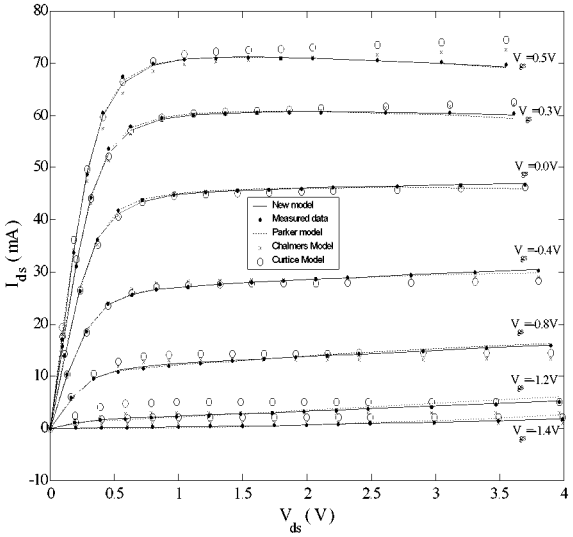

Fig. 1. Comparison of measured and modeled drain current characteristics of the new model, Parker model, Chalmers model, and Curtice model (wafer device).

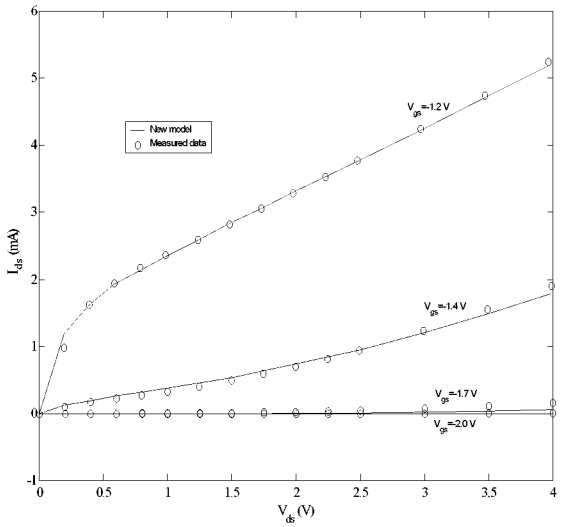

Fig. 2. Comparison of measured and proposed drain current characteristics around pinchoff region ($V_{\rm pinchoff} = -1.21$ V, wafer device).

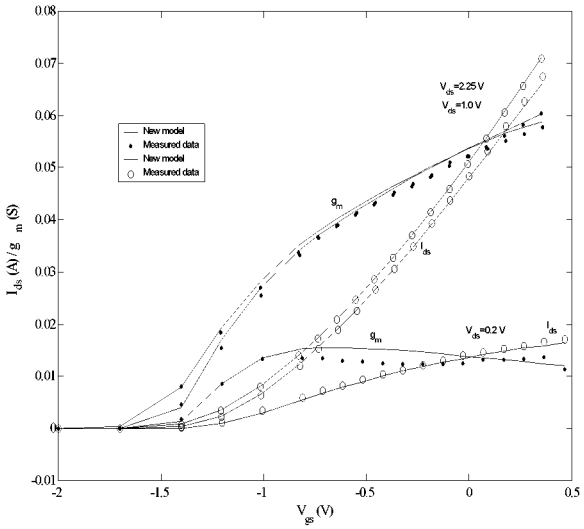

Fig. 3. Comparison of measured and simulated $I_{\rm ds}$–$V_{\rm gs}$ and g_m–$V_{\rm gs}$ characteristic based on the new model (wafer device).

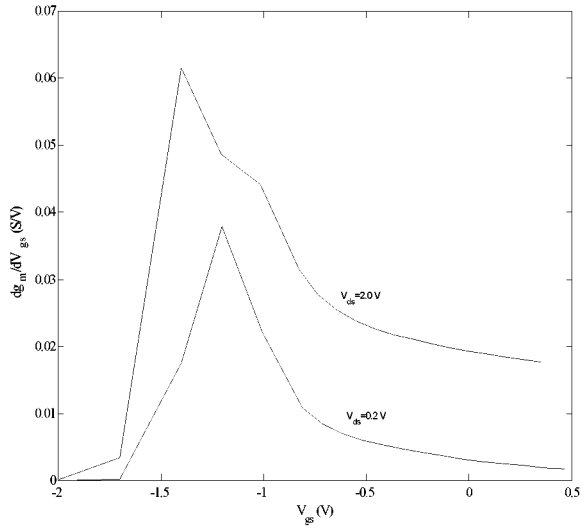

Fig. 4. Comparison of measured and simulated g_m characteristic close to pinchoff based on the new model (wafer device).

and 6 give the simulated $\partial g_m/\partial V_{\rm gs}$ versus $V_{\rm gs}$ and $\partial^2 g_m/\partial^2 V_{\rm gs}$ versus $V_{\rm gs}$ characteristics, respectively.

The maximum fitting error and the rms error of all models are listed in Table V for comparison. The calculation is made for five bias levels for $V_{\rm gs}$, while $V_{\rm ds}$ changes from 0.5 to 4.0 V (on-wafer device). As noted from Table V, both the maximum fitting error and the rms error are greatly reduced for the new model, as compared to the Curtice and Chalmers models. The maximum fitting error and rms error for both the Parker and new models are all very small. However, near the pinchoff condition ($V_{\rm gs} = -1.2$ V, $V_{\rm pinchoff} = -1.2$–1.21 V), the new model outperforms the Parker model. The newly proposed model contains more model parameters than the Curtice [1] and Chalmers models [2]. However, from the parameter-extraction procedure, there is no significant increase in simulation time required for the new model. This is because the new model only uses simple functions instead of a hyperbolic-tangent-type function, which

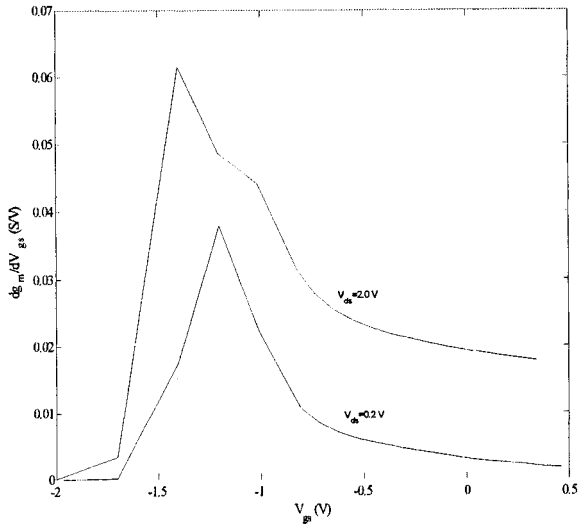

Fig. 5. Simulated $\partial g_m/\partial V_{\rm gs}$ versus $V_{\rm gs}$ characteristic.

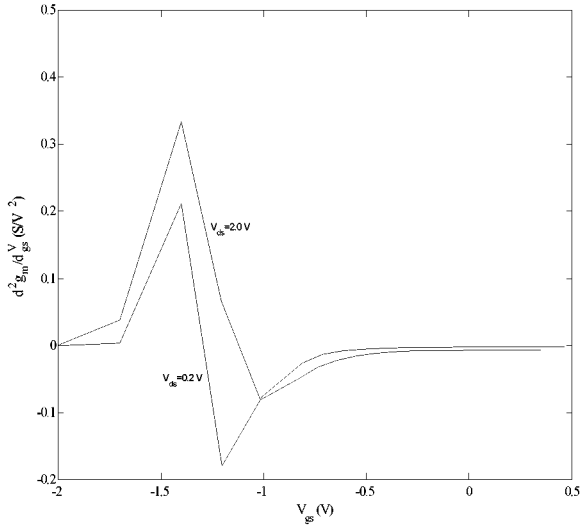

Fig. 6. Simulated $\partial^2 g_m/\partial^2 V_{\rm gs}$ versus $V_{\rm gs}$ characteristic.

TABLE V
COMPARISON OF THE MAXIMUM FITTING ERROR AND rms ERROR OF THE NEW MODEL WITH THE CURTICE, CHALMERS, AND PARKER MODELS (WAFER DEVICE)

Models		New Model	Parker Model	Curtice Model	Chalmers Model
V_{gs}=0.5V (V_{ds}=0.5-4.0V)	Max. Err. (%)	1.90	1.17	6.77	5.19
	RMS Err. (%)	0.78	0.55	3.26	2.71
V_{gs}=0.0V (V_{ds}=0.5-4.0V)	Max. Err. (%)	1.54	1.81	2.81	2.70
	RMS Err. (%)	0.50	0.72	1.48	1.08
V_{gs}=-0.5V (V_{ds}=0.5-4.0V)	Max. Err. (%)	0.56	1.46	7.73	6.13
	RMS Err. (%)	0.26	0.52	3.91	3.83
V_{gs}=-0.8V (V_{ds}=0.5-4.0V)	Max. Err. (%)	2.43	1.82	18.83	16.75
	RMS Err. (%)	1.20	1.00	11.14	8.78
V_{gs}=-1.2V (V_{ds}=0.5-4.0V)	Max. Err. (%)	1.31	17.89	146.8	45.47
	RMS Err. (%)	0.75	10.13	82.6	27.39

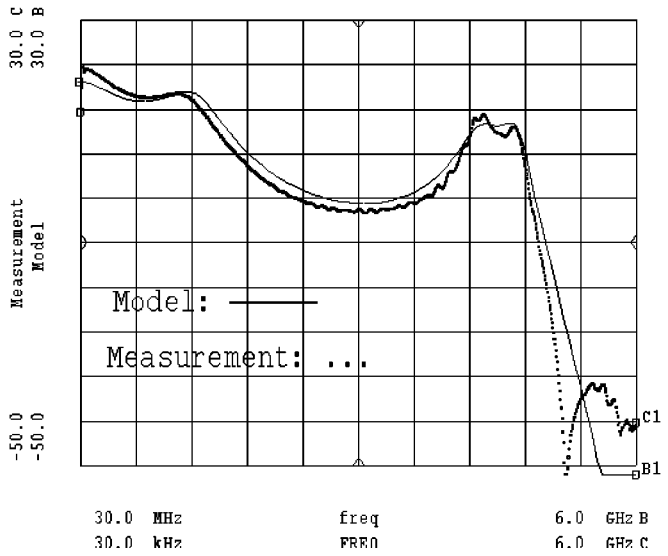

Fig. 7. Comparison of measured and simulated S_{21} of the amplifier.

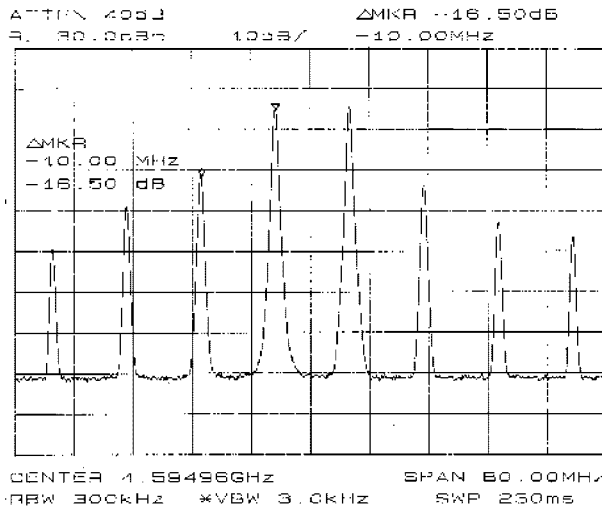

Fig. 8. Measured third-order intermodulation distortion of the amplifier ($P_{\text{in}} = 10$ dBm).

requires more simulation time and, most importantly, the model is continuous. The proposed model gives a comparable performance to the Parker model [5] and the number of model parameters is one less than the Parker model. The new model can be easily implemented in CAD software and could be very useful in microwave circuit simulation.

V. Amplifier Design Result With the New Model

A single-stage class-AB amplifier is designed and fabricated using Fujitsu FLC103WG to verify the performance of the new model. Good agreement was obtained. The amplifier is biased at $V_{\text{gs}} = -1.8$ V and $V_{\text{ds}} = 6.5$ V. The designed amplifier operates from 4.2 to 4.7 GHz with a gain of 10 dB. Both the S-parameters and third-order intermodulation distortions are measured and compared. The two-tone input signals are 4.5 and 4.51 GHz, respectively, and the input power is 10 dBm.

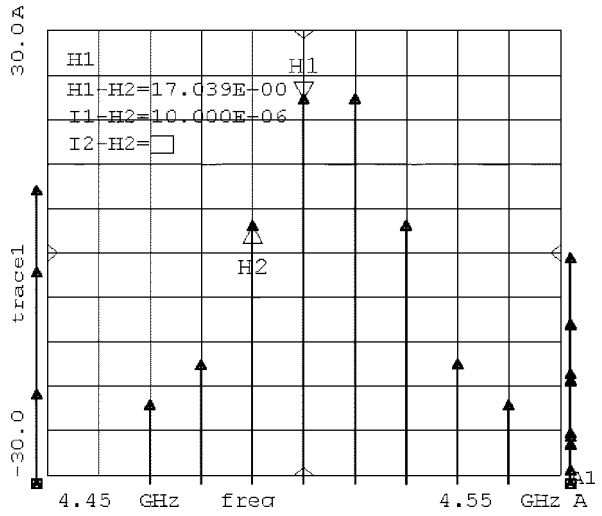

Fig. 9. Simulated third-order intermodulation distortion of the amplifier ($P_{\text{in}} = 10$ dBm).

Fig. 7 shows the measured and simulated S_{21} performance of the amplifier. Figs. 8 and 9 are the measured and simulated third-order intermodulation distortions, respectively. The simulated response and measured performance are in good accordance.

VI. Conclusions

An accurate large-signal model for GaAs MESFET has been proposed in this paper. The model is capable of accurately representing the actual device characteristics over an extended range of operation conditions. Model performance near the pinchoff region is greatly improved through the use of a special transformation for V_{gs}. Moreover, the model and its derivatives are continuous, which gives a smooth transition to different operation regions. The model equations only adopt simple functions, thus, the parameter extraction is simple. It can be a useful tool for modern communication and microwave circuits design.

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J. Y. Ma, photograph and biography not available at time of publication.

M. S. Leong (M'75–SM'98), photograph and biography not available at time of publication.